REMARKS

Claims 1-11 are pending. The Office Action dated July 13, 2004 in this Application has been carefully considered. The above amendments and the following remarks are presented in a sincere attempt to place this Application in condition for allowance. Claims 1, 5-7, 10 and 11 have been amended in this Response. Reconsideration and allowance are respectfully requested in light of the above amendments and following remarks.

An interview was held with the Examiner, Mr. John Trimmings, on October 12, 2004 to discuss the rejections under U.S.C. §103(a) and the proposed amendments thereto. Applicant thanks the Examiner for the courtesies extended.

Claim 10 stands rejected under 35 U.S.C. §112, second paragraph, as assertedly having a term that lacks a proper antecedent basis. Insofar as it may be applied against the Claim, this rejection is overcome because "the" has been deleted in line 8. Accordingly, Applicants respectfully requests that the rejection of Claim 10 under 35 U.S.C. § 112, second paragraph, be withdrawn.

Claims 1-11 stand rejected under 35 U.S.C. §103(a) in view of U.S. Patent No. 5,642,362 to Savir et al. ("Savir") and "Scan latch Design for Delay Test," Jacob Savir, 1997 Test Conference (IEEE Proceedings Intl.), Nov. 1-6, 1997, pp. 446-453 ("IEEE"). Insofar as they may be applied against the Claims, these rejections are overcome.

Rejected independent Claim 1 as now amended more particularly recites one of the distinguishing characteristics of the present invention, namely, "*a shift register latch (SRL) chain* and *a last* SRL connected to the combinatorial logic, *a* first SRL *of the SRL chain.*" (Emphasis added.) Support for this Amendment can be found, among other places, FIGURE 2 of the original Application.

Specifically, neither Savir nor IEEE disclose, teach, or suggest employing an SRL latch chain in combination with all other limitations of Claim 1. Specifically, Savir discloses a test circuit wherein XOR gates are employed, and IEEE shows a testing circuit that operates in a distributed manner. However, neither explicitly discloses a chain wherein logic interposed between at least some of the latches. By utilizing logic units between the at least some of the latches that are in a chain, better control of the test circuit can be achieved for a very large number inputs. By having such better control, which is not taught in either Savir or IEEE, more flexibility exists in testing that enables better performace and lower cost.

In view of the foregoing, it is apparent that the cited references do not disclose, teach or suggest the unique combination now recited in amended Claim 1. Applicants therefore submit that amended Claim 1 is clearly and precisely distinguishable over the cited reference in a patentable sense, and is therefore allowable over this reference and the remaining references of record. Accordingly, Applicants respectfully request that the rejection of Claim 1 under 35 U.S.C. § 103(a) in view of Savir and IEEE be withdrawn and that Claim 1 be allowed.

Claims 2-5 depend on and further limits Claim 1. Hence, for at least the aforementioned reasons, these Claims would be deemed to be in condition for allowance. Applicants respectfully request that the rejections of dependent Claims 2-5 also be withdrawn.

Rejected independent Claim 6 as now amended more particularly recites one of the distinguishing characteristics of the present invention, namely, "transmitting the first scan data bit from the logic unit to the second SRL if there is not a logic 1 signal [...and] transmitting the inverted bit of the first scan data bit from the logic unit to the second SRL if there is not the logic 1 signal." Support for this Amendment can be found, among other places, FIGURE 2 of the original Application.

Specifically, neither Savir nor IEEE disclose, teach, or suggest employing scan data to a logic unit that is interposed between at least some of the SRLs in combination with all other limitations of Claim 6. Specifically, Savir discloses a test circuit wherein XOR gates are employed, and IEEE shows a testing circuit that operates in a distributed manner. However, neither explicitly discloses a chain wherein logic interposed between at least some of the latches. By utilizing logic units between the at least some of the latches, better control of the test circuit can be achieved. By having such better control, which is not taught in either Savir or IEEE, more flexibility exists in testing that enables better performance and lower cost.

In view of the foregoing, it is apparent that the cited references do not disclose, teach or suggest the unique combination now recited in amended Claim 6. Applicants therefore submit that amended Claim 6 is clearly and precisely distinguishable over the cited reference in a patentable sense, and is therefore allowable over this reference and the remaining references of record. Accordingly, Applicants respectfully request that the rejection of Claim 6 under 35 U.S.C. § 103(a) in view of Savir and IEEE be withdrawn and that Claim 6 be allowed.

Claims 7-9 depend on and further limits Claim 6. Hence, for at least the aforementioned reasons, these Claims would be deemed to be in condition for allowance. Applicants respectfully request that the rejections of dependent Claims 7-9 also be withdrawn.

Applicants respectfully contend that the rejection of Claims 10 and 11 are overcome for at least some of the reasons that the rejection of Claim 6 as amended is overcome. These reasons include neither Savir nor IEEE disclosing, teaching, or suggesting "transmitting the first scan data bit from a logic unit to a second SRL if there is not a logic 1 signal." Applicants therefore respectfully submit that amended Claims 10 and 11 are clearly and precisely distinguishable over the cited references in any combination.

In view of the foregoing, it is apparent that the cited references do not disclose, teach or suggest the unique combination now recited in amended Claims 10 and 11. Applicants therefore submit that amended Claim 10 is clearly and precisely distinguishable over the cited reference in a patentable sense, and is therefore allowable over this reference and the remaining references of record. Accordingly, Applicants respectfully request that the rejection of Claims 10 and 11 under 35 U.S.C. § 103(a) in view of Savir and IEEE be withdrawn and that Claim 10 be allowed.

Applicants have now made an earnest attempt to place this Application in condition for allowance. For the foregoing reasons and for other reasons clearly apparent, Applicants respectfully request full allowance of Claims 1-11.

Applicants do not believe that any fees are due; however, in the event that any fees are due, the Commissioner is hereby authorized to charge any required fees due (other than issue fees), and to credit any overpayment made, in connection with the filing of this paper to Deposit Account No. 50-0605 of CARR LLP.

Should the Examiner require any further clarification to place this application in condition for allowance, the Examiner is invited to telephone the undersigned at the number listed below.

Respectfully submitted,

CARR LLP

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